REMARKS

Claims 1-67 were pending in the above-identified application. Of these, claims 1, 2, 4-7, 9-14, 16-35, 37-40, 42-44, 46-50, 52, 53, and 63-67stand rejected; and claims 3, 8, 15, 36, 41, 45, 51, and 54-62 are objected to. Applicants, having amended the application, respectfully request reconsideration.

Rejections Under 35 U.S.C. §112

Claims 18, 26, 53 and 66 stand rejected under section 112, second paragraph, "as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention" (office action, page 6). Applicants have amended claims 18, 26, 53, and 66 to address problems of antecedent basis identified by the examiner. Applicants thank the examiner for her extraordinary attention to detail.

Rejections Under 35 U.S.C. §102

Claim 1

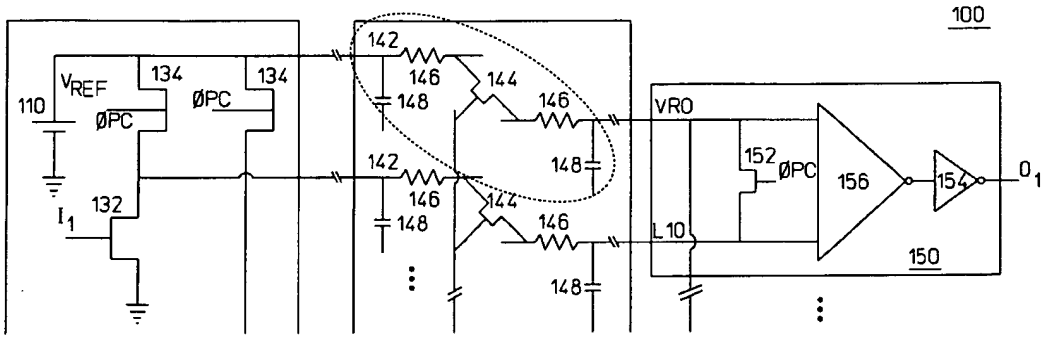
Claim 1 stands rejected under Perner (US Pat. No. 5,818,261). In particular, the examiner believes the circuit of Perner's figure 1 depicts each element of the apparatus of claim 1. Applicants respectfully disagree.

Claim 1 recites "a reference receiver that receives [a] common reference voltage...and in response *produces a buffered voltage* that is derived at least in part from the common reference voltage..." (emphasis added). The examiner finds support for the recited "reference receiver" in the interconnect network 140 in Perner's figure 1 (office action, page 7). Consistent with this view, the examiner cites node V_{REF} as meeting the common reference voltage and the voltage on node V_{R0} as meeting the "buffered voltage" of claim 1. The interpretation of Perner is incorrect: the signal on node V_{R0} is not a "buffered" voltage.

Applicants' specification correctly identifies buffers as amplifiers (specification, page 6, line 15). In the lexicon of electrical engineers, a "buffer" is an amplifier with high input

impedance and low output impedance.[1] Amplifiers called "voltage followers" are commonly used as buffers.[2] Simple voltage followers, and thus simple buffers, can be formed using either bipolar or FET transistors. Those based upon bipolar transistors are alternatively termed "common collector" or "emitter follower" amplifiers, while those based upon FET transistors are alternatively termed "common source" or "source follower" amplifiers. Consistent with this terminology, applicants identify one embodiment of the invention as using MOSFET-based source-followers as a buffer (specification, page 8, lines 13-15). The production of a "buffered voltage" from a "common reference voltage," as required in claim 1, thus requires the common reference voltage be presented on a high-impedance node and the buffered voltage be presented as an amplified signal on a low-impedance node. (In an ideal voltage follower, the output voltage is the same as the input voltage. Voltage followers are nevertheless "amplifiers" because the output current is greater than the input current.)

The examiner argues that elements 142, 144, 146, and 148 of Perner's Fig. 1 meet the "reference receiver" of claim 1 and produce "a voltage VR0" as the buffered voltage (office action, page 7). A portion of Perner's Fig. 1 is reproduced below for ease of review. A dotted line encircles the elements the examiner identifies as producing a "buffered voltage" VR0.



Portion of Perner's Fig. 1

Node VR0 is coupled to reference voltage VREF via a switch 144 and a pair of resistors

1 *See* "Electronics Circuits and Devices," 2nd Ed., by Ralph J. Smith (1980), p. 442; and "The Essence of Analog Electronics," by Colin Lunn (1997), pp. 78, 79, and 211.
2 *Ibid.*

142 and 146. These components are not arranged as an amplifier at all, much less a buffer, and cannot produce a "buffered voltage." Just the opposite, Perner's cross point switches attenuate voltage V_{REF}, though this attenuation is apparently kept to a minimum: Perner uses a low reference voltage V_{REF}, and as a result reports that "very little signal *will be lost* through the NMOS cross point switches" (Perner, 6:15-20, emphasis added). Perner's voltage VR0 is therefore an *attenuated* version of reference voltage V_{REF}, and thus cannot be considered a "buffered" voltage.

In summary, interconnect network 140 of Perner is not a receiver, and cannot produce buffered voltages. Instead, interconnect network 140 is made up of passive circuit elements "e.g. resistors and capacitors" and a series of cross point switches 144 that together attenuate voltage V_{REF} to produce the distributed voltage VR0. Because the cross point switches and related components are not receivers and do not produce "buffered voltages," Perner does not anticipate claim 1. The rejection of claim 1 over that reference should therefore be withdrawn.

Claims 2, 4-7, 9-13, and 16-18

Claims 2, 4-7, 9-13, and 16-18, depend from claim 1, and consequently distinguish Perner for at least the same reasons claim 1 distinguishes. The rejections of these claims should therefore be withdrawn.

Claim 19

Claim 19 recites "a reference buffer that receives the common reference voltages and in response produces a buffered referenced voltage..." As noted above in connection with the discussion of claim 1, Perner does not include buffers for developing voltage VR0: just the opposite, voltage VR0 is an attenuated version of reference voltage V_{REF}. Perner's network 140 thus cannot be considered a "buffer," nor can voltage VR0 be considered a "buffered voltage." The rejection of claim 19 should therefore be withdrawn.

Claim 20-24, 27, and 28

Claims 20-24, 27, and 28 depend from claim 19, and consequently distinguish Perner for at least the same reasons claim 19 distinguishes. The rejections of these claims should therefore be withdrawn.

Claim 29

Claim 29 recites, among other things, "a second integrated circuit that receives [a] common referenced voltage... having a *reference buffer* that receives the common referenced voltage and in response produces a buffered referenced voltage..." (emphasis added). The examiner again finds support for the buffer and buffered voltage in crossconnect switches 144 of Perner's interconnect network 140. As noted above, interconnect network 140 is not a buffer, does not include a buffer, and does not produce buffered voltages. The rejection of claim 29 over Perner should therefore be withdrawn.

Claims 31-33, 37, and 38

Claims 31-33, 37, and 38, depend from claim 29, and consequently distinguish Perner for at least the same reasons claim 29 distinguishes. The rejections of these claims should therefore be withdrawn.

Claim 39

Claim 39 recites a method that includes "receiving pseudo-differential signaling that includes a common reference voltage" and "*producing a buffered voltage based at least in part on the common reference voltage...*" (emphasis added). The examiner again finds support for the buffered voltage in crossconnect switches 144 of Perner's interconnect network 140. As noted above, interconnect network 140 is not a buffer, does not include a buffer, and does not produce buffered voltages. The rejection of claim 39 over Perner should therefore be withdrawn.

Claims 40, 42-44, 48, 49, 52, and 53

Claims 40, 42-44, 48, 49, 52, and 53, depend from claim 39, and consequently distinguish Perner for at least the same reasons claim 39 distinguishes. The rejections of these claims should therefore be withdrawn.

Claim 63

Claim 63 recites a system that includes "a reference receiver that receives [a] common reference voltage and in response produce a buffered voltage..." the examiner finds support for the buffered reference voltage in reference voltage VR0 of Perner's figure 1 (office action, pages 10 and 11). For reasons similar to those discussed above, voltage VR0 is not buffered, nor is interconnect network 140 a buffer circuit. The rejection of claim 63 as anticipated by Perner should therefore be withdrawn.

Claims 64-67

Claims 64-67, depend from claim 63, and consequently distinguish Perner for at least the same reasons claim 39 distinguishes. The rejections of these claims should therefore be withdrawn.

Rejections Under 35 U.S.C. §103(a)

Claims 14, 25, 30, 35, 46, 47, and 50 stand rejected under section 103(a) as unpatentable over Perner in view of Boudry (US Pat. No. 5,644,254) Claim 14 depends from claim 1, and thus includes the buffered reference voltage. In rejecting claim 14, the examiner relies upon referenced voltage VR0 of Perner's figure 1 to meet the requisite "buffered voltage." Perner does not include a buffered referenced voltage, however, and so the combination presented by the examiner fails to recite each element of claim 1 and dependent claim 14. Because the references, taken in separately or in combination, do not include all the elements of claim 14, the rejection of claim 14 should be withdrawn.

Claim 25 depends from claim 19, and recites the specific case in which "the referenced buffer has a bandwidth that is greater than the residents input frequency" of a "plurality of signal inputs." The interconnect network 140 of Perner that the examiner relies upon to meet the requirement of "a referenced buffer" is not a buffer at all. In failing to include every element of the claims, the combination proposed by the examiner fails to establish a *prima facie* case of obviousness. The rejection of claim 25 should therefore be withdrawn.

Claims 30 and 35 depend from claim 29, and consequently recite a reference buffer that produces a buffered referenced voltage. The examiner's characterization of Perner as including such a reference buffer and reference voltage is in error, and so fails to establish a *prima facie* case of obviousness. The rejection of claims 30 and 35 should therefore be withdrawn.

Each of claims 46, 47, and 50 depends from claim 39, and consequently recites the step of "producing a buffered voltage based at least in part on [a] common reference voltage..." Voltage VR0 of Perner, which the examiner relies upon to meet the requirement of a "buffered voltage," is not in fact buffered, and consequently fails to meet that requirement. In the absence of each element of claim 39, claim 39 and its dependencies cannot be considered obvious over the cited references. The rejections of claims 46, 47, and 50 should therefore be withdrawn.

Claim 34 stands rejected under section 103(a) as unpatentable over Perner in view of Sessions (US Pat. No. 5,994,925). Once again, the examiner's assessment of Perner as including

the recited "buffered voltage" is incorrect, so the examiner's argument fails to establish a *prima facie* case of obviousness.

Allowable Subject Matter

Claims 3, 8, 15, 36, 41, 45, and 51 are objected to as being dependent upon rejected base claims. The examiner would consider them allowable however if rewritten in independent form to include the limitations of the base claim and any intervening claims (office action, page 12). Applicants have noted above, however, that the rejections of the independent claims are based upon an incorrect reading of Perner. Applicants therefore elect not to amend the claims the examiner deemed to be allowable.

CONCLUSIONS

In light of the foregoing remarks and amendments, the pending claims are in condition for allowance; accordingly, Applicants' respectfully request a Notice of Allowance. If the Examiner's next action is other than the allowance of the pending claims, the Examiner is requested to call Applicants' attorney at (925) 621-2113.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Amenedment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 9/27/05

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Signature